

Abstract of the Disclosure

A ferroelectric memory cell for use in a ferroelectric random
5 access memory (FeRAM) device that includes a first active area
incorporating therein a gate of a depletion mode transistor, a
second active area adjacent to the first active area and
incorporating therein a gate of an enhancement mode transistor, a
word line coupled to the gate of the depletion mode transistor and
10 the gate of the enhancement mode transistor, and a ferroelectric
capacitor coupled to a drain of the enhancement mode transistor,
for storing data.

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